**REMARKS**

**Introduction**

Claims 3, 5-8, 11-14, 21, 23-26, 30-32, 37, 38, and 49-52 have been amended. Claims 1, 2, 10, 19, 20, 28, and 39-48 have been cancelled. The Applicants request entry of this Rule 116 Response.

Support for amended claims 3 and 21 is found in, for example, prior claims 10 and 28, and Figs. 8 and 9; pg. 10, line 22 - pg. 11, line 3; pg. 18, lines 8-15; and pg. 46, lines 12-21.

Claims 5-8, 11-14, 49, and 50 have been amended to depend from claim 3. Claims 23-26, 30-32, 37, 38, 51, and 52 have been amended to depend from claim 21. Claims 7, 8, and 25 have been amended to provide explicit antecedent support for "***the*** rate of change." Claims 23 and 24 have been amended to address the antecedent basis issue identified by the Examiner.

Care has been taken to avoid the introduction of new matter.

**Priority**

The Office Action Summary does not acknowledge the Applicants' request for foreign priority under U.S.C. § 119(a)-(d).

The Applicants respectfully request of their claim for foreign priority under U.S.C. § 119(a)-(d).

Copies of the International Application for priority under 35 U.S.C. § 371 (c)(2) and a foreign search report PCT/ISA/210 with the accompany cited references cited in Information

Disclosure Statements (IDS) were filed on March 24, 2006 along with the corresponding fees. Receipt of these documents was acknowledged by the USPTO in a stamped postcard. An executed declaration under 35 U.S.C. § 371 (c)(4) was filed by the Applicants on May 15, 2006. Receipt of the executed declaration was acknowledged by the USPTO in a stamped postcard.

Further, the USPTO issued a Notice of Acceptance of Application Under 35 U.S.C. § 371 (c)(1), (c)(2), and (c)(4) and 37 C.F.R. 1.495 on May 15, 2006. The Notice of Acceptance acknowledged the copy of the International Application (IA), English translation of the IA, copy of the International Search Report, IDS, Declaration, Request for Immediate Examination, and U.S. Basic National Fees.

Accordingly, the Applicants submit that this application is a National Stage Application under 35 U.S.C. § 371 and fully comports with 35 U.S.C. § 119(a)-(d). The Applicants respectfully request the acknowledgement of their claim for foreign priority under U.S.C. § 119(a)-(d) in the next Office Action.

**Claim Rejection Under 35 U.S.C. § 112**

Claims 23 and 24 are rejected under 35 U.S.C. § 112, second paragraph, as purportedly being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention.

Claims 23 and 24 have been amended, as suggested by the Examiner.

Withdrawal of the foregoing rejections is respectfully requested.

**Claim Rejection Under 35 U.S.C. § 102**

Claims 1-3, 5, 7-21, 23, 25-36, 38, and 49-57 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,346,581 to Tsang.

Applicant traverses.

An aspect of amended claims 3 and 21 is a cleaning treatment method of a semiconductor layer where an absolute value for a rate of change in thickness of the semiconductor layer during the cleaning treatment step is 0.1 nm/sec or less.

With respect to claims 10 and 28, the Examiner contends that Tsang discloses that the rate of change in thickness is 0.1 nm/sec or less. The Examiner avers that the etch rate of Tsang can be adjusted to about 0.53 nm/sec, which equals about 2 μm/hr, which would result in the rate of change of 0.1 nm/sec or less.

Tsang states in col. 5, lines 60-64:

> [t]he wafer was heated to 545°C and the wafer surface was exposed to a beam of $PCl_3$ and TMIn ($PCl_3$ flow rate equivalent to 1.1 nm/s etch rate; TMIn flow rate equivalent to 0.1 nm/s growth rate) for approximately 45 minutes.

An aspect of the present invention is a method of cleaning a semiconductor layer where etching gas and growth gas are supplied simultaneously and the supply of both gases is stopped simultaneously. Another aspect of the present invention includes a period of time where neither the etching gas nor growth gas is supplied.

On the other hand, Tsang discusses providing a growth gas without supplying the etching gas after supplying the etching gas and growth gas simultaneously (*see, e.g.,* col. 5, lines 49-68 and col. 6, lines 1-17). Tsang's step of supplying the growth gas without supplying the etching gas provides an opposite effect to the residual buried Silicon (Si) in contrast to the present invention.

Tsang fails to disclose or suggest, at a minimum, an absolute value for a rate of change in a thickness of the semiconductor layer during the cleaning treatment step ***is 0.1 nm/sec or less***, as required by amended claims 3 and 21.

Tsang describes a $PCl_3$ flow rate equivalent to 1.1 nm/s etch rate and a TMIn flow rate equivalent to 0.1 nm/s growth rate (*see, e.g.,* col. 5, lines 62-64). Thus, the rate of change in the thickness of the semiconductor layer during the cleaning treatment step of Tsang is 1.0 nm/sec (value of 1.0 nm/sec = −1.1 nm/sec + 0.1 nm/sec). Therefore, Tsang describes R equal to 1.0 nm/sec, not 0.1 nm/sec or less.

Also, Tsang describes that 2 μm/hr is the growth rate of re-growth process after the cleaning treatment process. Therefore, Fig. 2 of Tsang does not show that the etch rate can be adjusted to about .53 nm/sec (about 2μm/hr) of re-growth rate, which would result in R being 0. 1 nm/sec or less.

Further, Tsang *teaches away* from adjusting the flow between etch gas and growth gas by switching between net deposition and net removal (*see, e.g.,* col. 5, lines 10-12). Tsang describes that etching generally results in smooth and texture-less surface at etch rates ≤ 0.6 nm/s, which would result in $|R|$ equal to 0.1 nm/sec or less (col. 4, lines 36-53).

Thereby as taught in the instant specification, when R is 0.1 nm/sec or less and the etch gas and growth gas is supplied in an intermittent manner, the concentration of residual Si is markedly reduced (*see, e.g.,* Fig. 8 of the originally filed specification).

With respect to claim 53, the Office Action asserts that Tsang discloses that the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness is $|R| < |r_2| < |r_1|$.

Tsang discusses that $r_1$ is -1.1 nm/s (etch rate) and $r_2$ is +0.1 nm/s (growth rate) (*see, e.g.,* col. 5, lines 62-64). Accordingly, the value of $|R|$ in Tsang is 1.0 nm/s because of

$|R| = r_1 + r_2$. Therefore, Tsang describes $|r_2=+0.1$ nm/s$| < |R= -1.0$ nm/s$| < |r_1= -1.1$ nm/s$|$. The value of $|R|$ in the present invention is negative, not positive. Therefore, the cleaning treatment method according to the present invention makes the thickness of the semiconductor layer decrease. Thus, Tsang fails to disclose or suggest, the amount of the first gas and the second gas supplied is adjusted in such a manner than an absolute value for the rate of change of layer thickness becomes $|R| < |r_2| < |r_1|$, as required by claim 53.

Dependent claims 5, 7-9, 11-18, 23, 25-27, 29-36, 38, and 49-52, and 54-57 are allowable for at least the same reasons as their respective base claim, and further distinguish the claimed method of manufacturing a semiconductor device.

With respect to dependent claims 5 and 55, Tsang does not disclose the technical feature that "a difference in layer thickness of the semiconductor layer before and after implementation of the cleaning treatment step is 100 nm or less". Tsang states in col. 5, lines 64-66:

> This resulted in removal of the unmasked material to below the substrate/lower cladding layer interface.

Thus, Tsang describes removing the upper cladding layer (1.5 μm), the active layer (0.1 μm) and the lower InGaAsP cladding layer (1.0 μm) (*see, e.g.,* column 5, lines 51-55). Tsang discusses removing more than 2.6 μm (1.5 μm + 0.1 μm + 1.0 μm) of the unmasked material. Further, Tsang discloses R that

1.0 nm/sec (1.0 nm/sec = -1.1 nm/sec + 0.1 nm/sec) for 45 minutes (*see, e.g.,* col. 5,lines 62-64).

Accordingly, Tsang discloses that a difference in the layer thickness of the semiconductor layer before and after implementation of the cleaning treatment step is about 2.7 μm. Incidentally, the Silicon carbide ($SiC_2$) layer on the upper cladding layer is not removed during the cleaning treatment process because the $SiC_2$ layer functions as mask.

Dependent claim 50 recites, in part, "…a concentration of residual Si of said surface of said semiconductor layer is a surface density of $2.5 \times 10^{11}$ atoms/$cm^2$ or less." Tsang is *silent* regarding this feature. Further, in the related Japanese Patent No. 4,186,489, this claim, which is presented as claim 57 has been allowed.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities," *Scaltech Inc. v. Retec/Tetra,* 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission,* 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Tsang does not anticipate amended claims 3, 21, and 53 nor any claim dependent thereon.

**Claim Rejections Under 35 U.S.C. § 103**

Claims 4 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsang.

Claims 6, 24, and 37 are rejected under 35 U.S.C. §103(a) as being unpatentable over Tsang in view of U.S. Patent No. 5,946,582 to Bhat.

Dependent claims 4, 6, 24, and 37 are allowable for at least for the same reasons as their respective base claim, and further distinguish the claimed cleaning treatment method.

With respect to dependent claims 6 and 24, the thickness of a semiconductor layer is not substantially reduced in Bhat because Bhat only slightly etches the surface by wet-etching to decrease a capacitance of Heterojunction bipolar transistors (HBT), not to eliminate the residual impurities within the surface. Therefore, Bhat is unable to attain claimed difference in layer thickness of the semiconductor layer even if a technical feature of Bhat is added to a method of Tsang. Bhat does not cure the deficiencies of Tsang

As Tsang and Bhat do not disclose the same cleaning treatment method as disclosed by the present inventors, and even if combined still fail to disclose or suggest the elements recited by amended claims 3 and 21, the combination of Tsang and Bhat does not render the method as recited by amended claims 3 and 21 obvious.

Withdrawal of the foregoing rejections is respectfully requested.

**Conclusion**

Entry of the above amendments is earnestly solicited. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Should there be any matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

This response is believed to be fully responsive and to put the case in condition for allowance. An early and favorable action on the merits is earnestly requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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